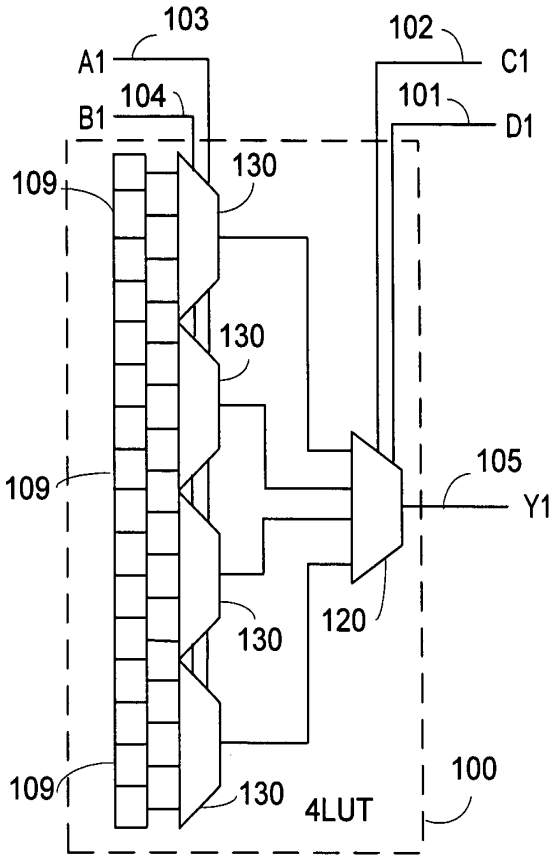



**FIG. 1. Lookup Table and LUT Mask**

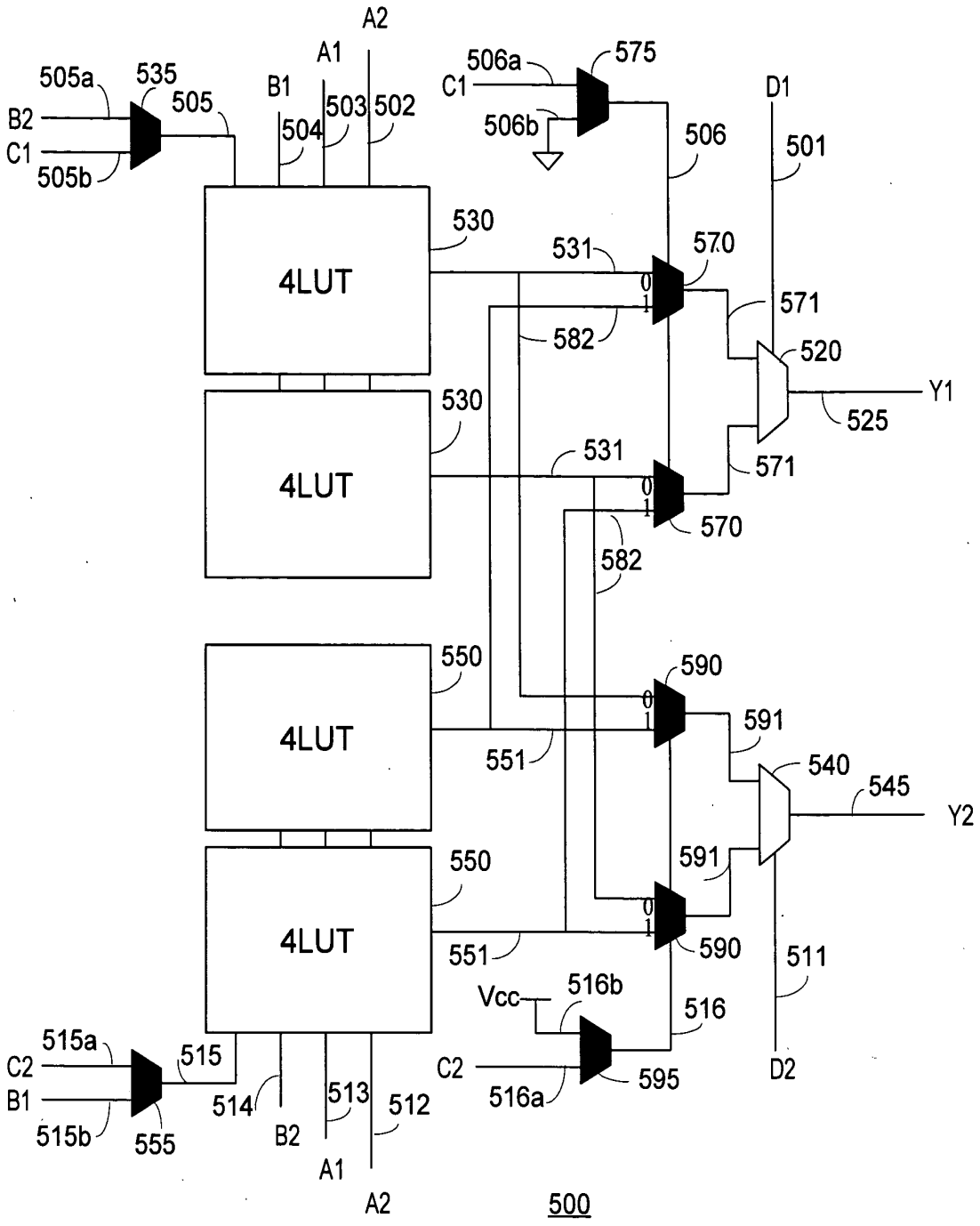



**FIG. 2. Shared Lookup-Table Mapping Circuitry**

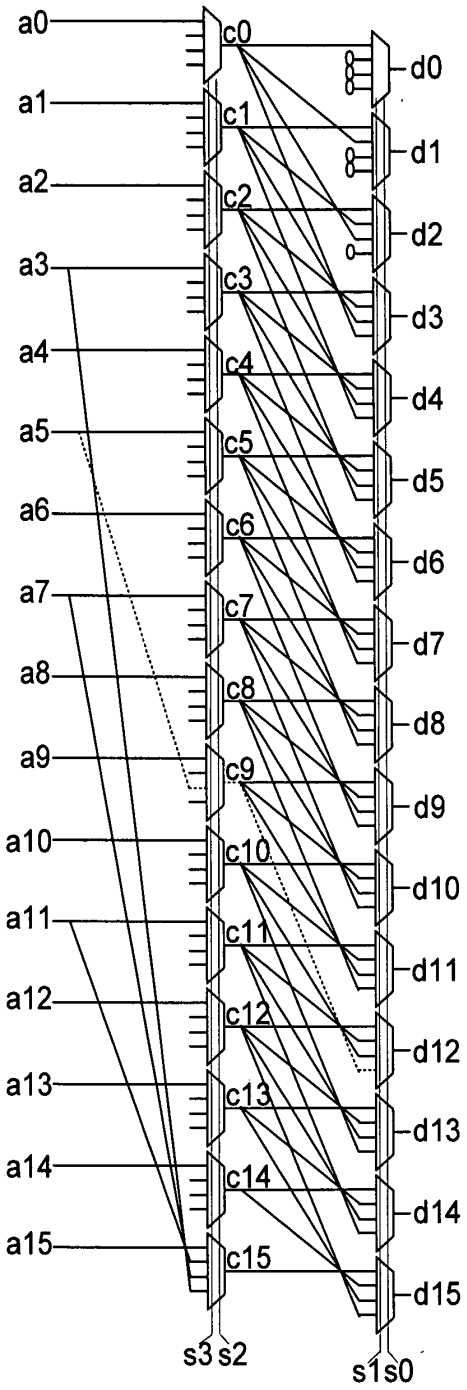



**FIG. 3a. 16x16 non-rotational barrel shifter (some connections removed). Note that a[i] inputs can be arbitrary width busses.**

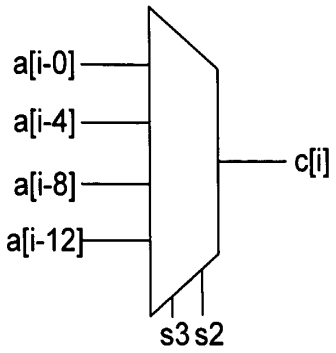



**FIG. 3b. Generalized Stage 1**

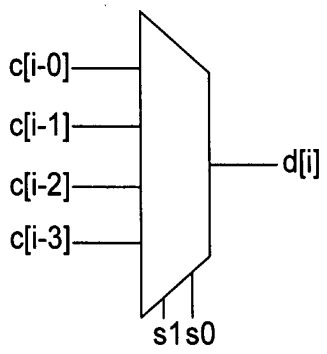



**FIG. 3c. Generalized Stage 2**

Example: When {s3,s2,s1,s0} = {0111} stage 1 reaches back 4 bits, and stage 2 reaches back 3 bits for a total of 7. Thus the output is {0,0,0,0,0,0,0,a0,a1,a2,a3,a4,a5,a6,a7,a8}.

Illustrated is the connected path for a5 to c9 to d12 for these settings.

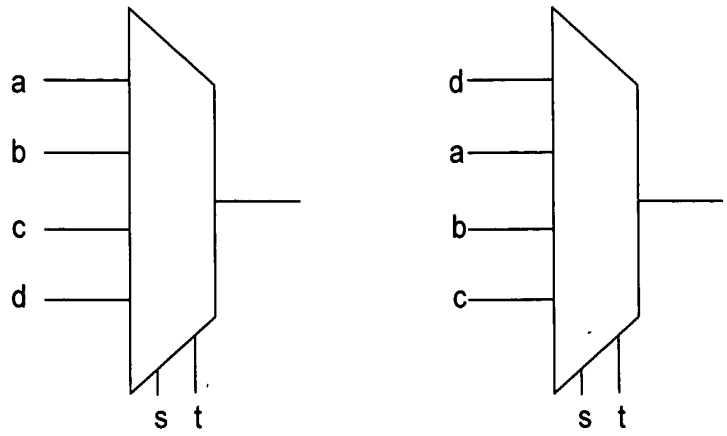



**FIG. 4a. 4:1 muxes incompatible with SLM**

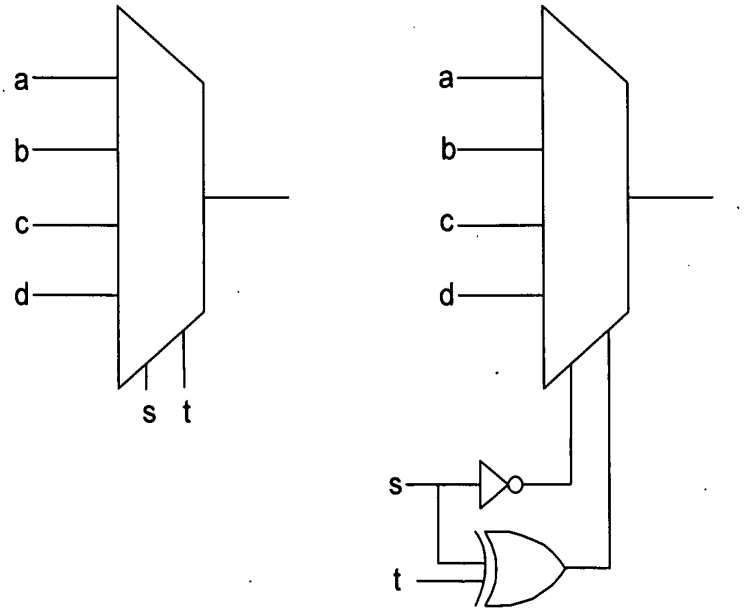



**FIG. 4b. 4:1 muxes made compatible with manipulation of the select bits.**

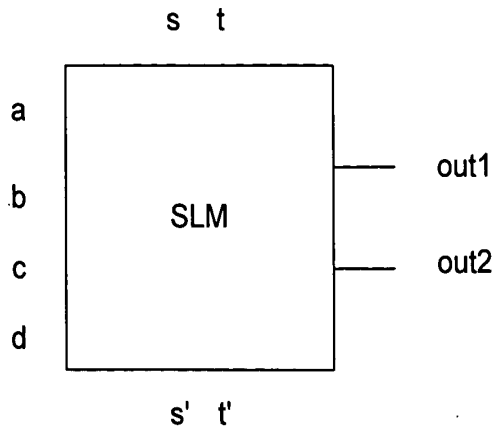



**FIG. 5. Notation used to describe two 4:1 muxes with same data and different select lines implemented using SLM.**

| | "-12" | "-8" | "-4" | "0" | | SLM PAIRS |
|---|---|---|---|---|---|---|
| c0 = mux( | *a4,* | *a8,* | *a12,* | a0; | s2, s1) | c0, c4 |
| c1 = mux( | *a5,* | *a9,* | *a13,* | a1; | s2, s1) | c1, c5 |
| c2 = mux( | *a6,* | *a10,* | *a14,* | a2; | s2, s1) | c2, c6 |
| c3 = mux( | *a7,* | *a11,* | *a15,* | a3; | s2, s1) | c3, c7 |
| c4 = mux( | *a8,* | *a12,* | *a0,* | a4; | s2, s1) | |
| c5 = mux( | a9, | *a13,* | a1, | a5; | s2, s1) | |
| c6 = mux( | *a10,* | *a14,* | a2, | a6; | s2, s1) | |
| c7 = mux( | *a11,* | *a15,* | a3, | a7; | s2, s1) | |
| c8 = mux( | *a12,* | *a0,* | a4, | a8; | s2, s1) | c8, c12 |
| c9 = mux( | *a13,* | a1, | a5, | a9; | s2, s1) | c9, c13 |
| c10 = mux( | *a14,* | a2, | a6, | a10; | s2, s1) | c10, c14 |
| c11 = mux( | *a15,* | a3, | a7, | a11; | s2, s1) | c11, c15 |
| c12 = mux( | a0, | a4, | a8, | a12; | s2, s1) | |
| c13 = mux( | a1, | a5, | a9, | a13; | s2, s1) | |
| c14 = mux( | a2, | a6, | a10, | a14; | s2, s1) | |
| c15 = mux( | a3, | a7, | a11, | a15; | s2, s1) | |

| | "-3" | "-2" | "-1" | "0" | |
|---|---|---|---|---|---|
| d0 = mux( | *c13,* | *c14,* | *c15,* | c0; | s2, s1) |
| d1 = mux( | *c14,* | *c15,* | c0, | c1; | s2, s1) |
| d2 = mux( | *c15,* | c0, | c1, | c2; | s2, s1) |
| d3 = mux( | c0, | c1, | c2, | c3; | s2, s1) |
| d4 = mux( | c1, | c2, | c3, | c4; | s2, s1) |
| d5 = mux( | c2, | c3, | c4, | c5; | s2, s1) |
| d6 = mux( | c3, | c4, | c5, | c6; | s2, s1) |
| d7 = mux( | c4, | c5, | c6, | c7; | s2, s1) |
| d8 = mux( | c5, | c6, | c7, | c8; | s2, s1) |
| d9 = mux( | c6, | c7, | c8, | c9; | s2, s1) |
| d10 = mux( | c7, | c8, | c10, | c10; | s2, s1) |
| d11 = mux( | c8, | c9, | c10, | c11; | s2, s1) |
| d12 = mux( | c9, | c10, | c11, | c12; | s2, s1) |
| d13 = mux( | c10, | c11, | c12, | c13; | s2, s1) |
| d14 = mux( | c11, | c12, | c13, | c14; | s2, s1) |
| d15 = mux( | c12, | c13, | c14, | c15; | s2, s1) |

**FIG. 6. SLM pairings allowable with maniuplation of select bits.**

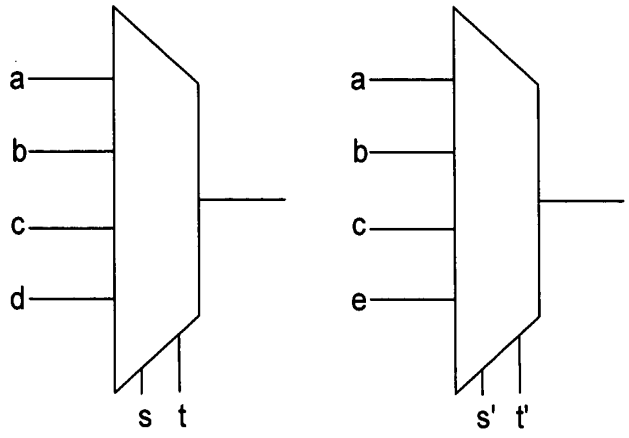



**FIG. 7a. 4:1 muxes incompatible with SLM**

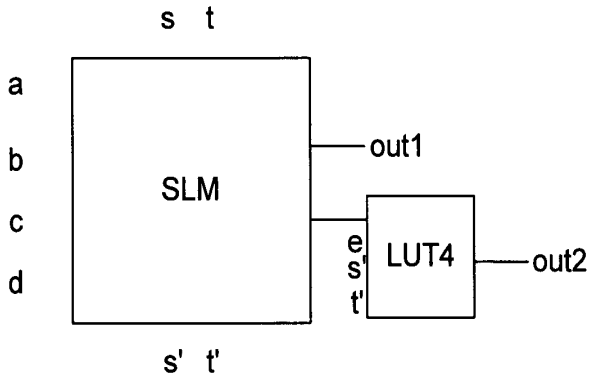



**FIG. 7b. 4:1 muxes made compatible with a "repair" logic element.**

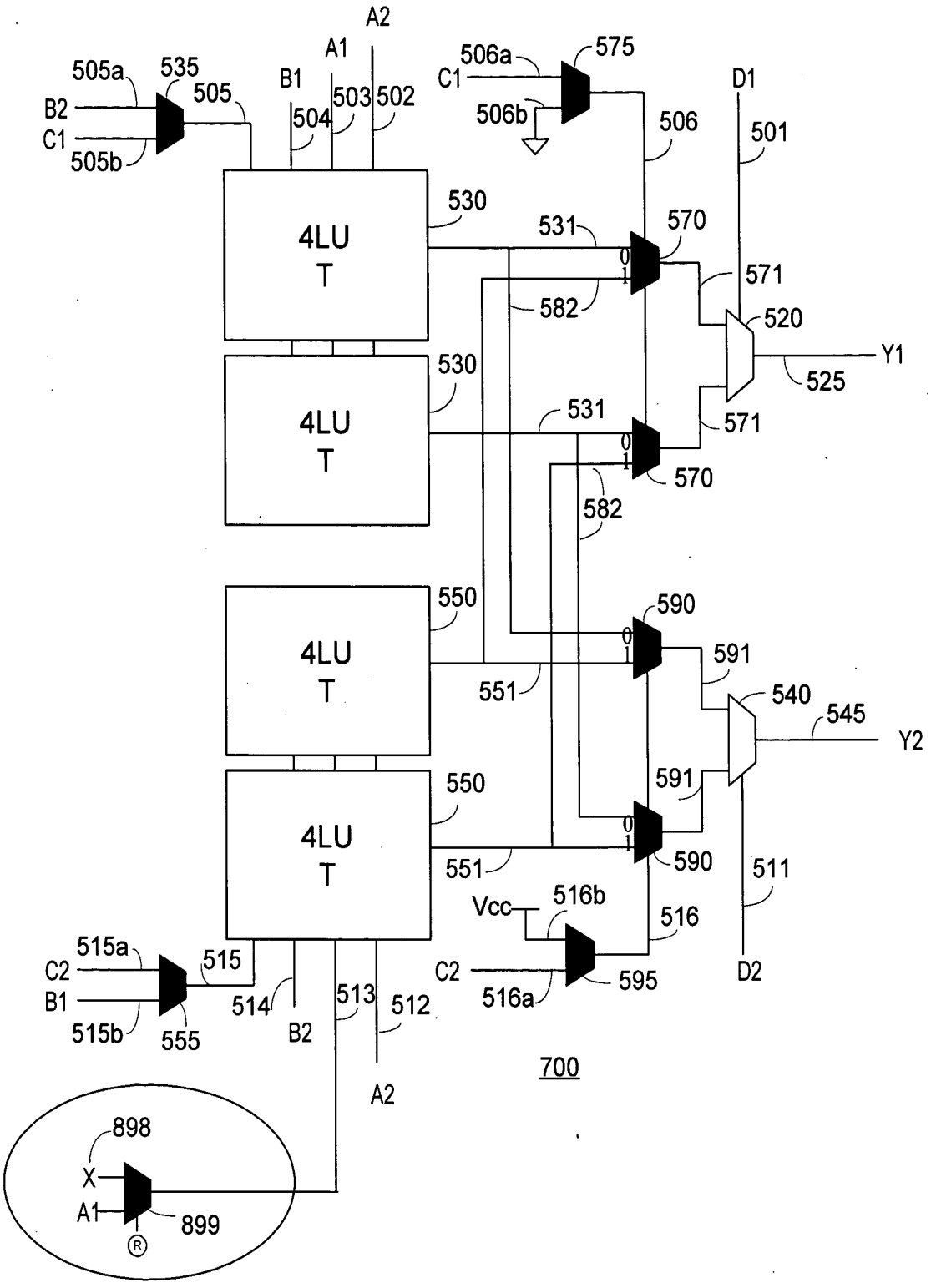



**FIG. 8. Shared Lookup-Table Mapping Circuitry with Additional Input**

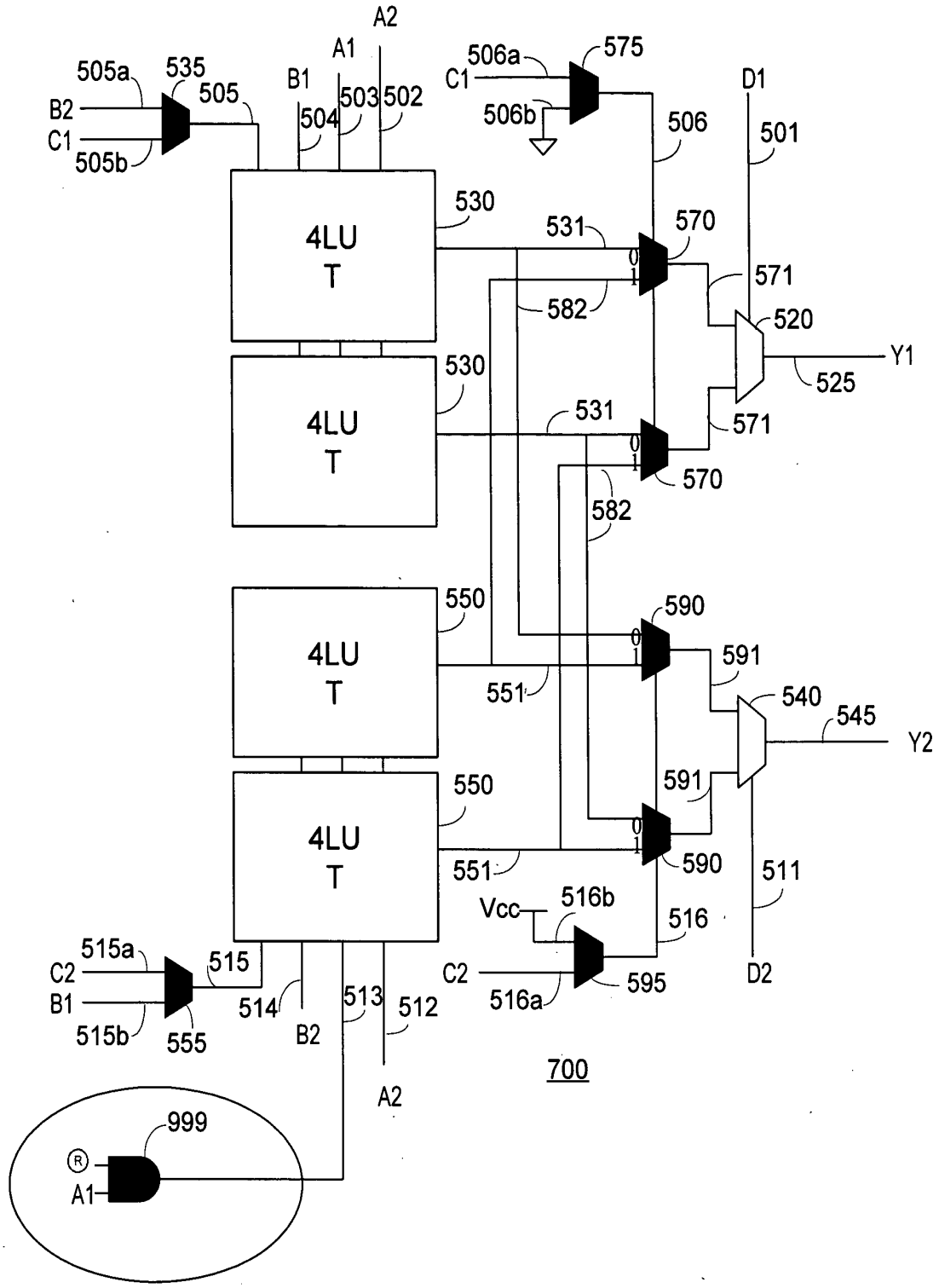
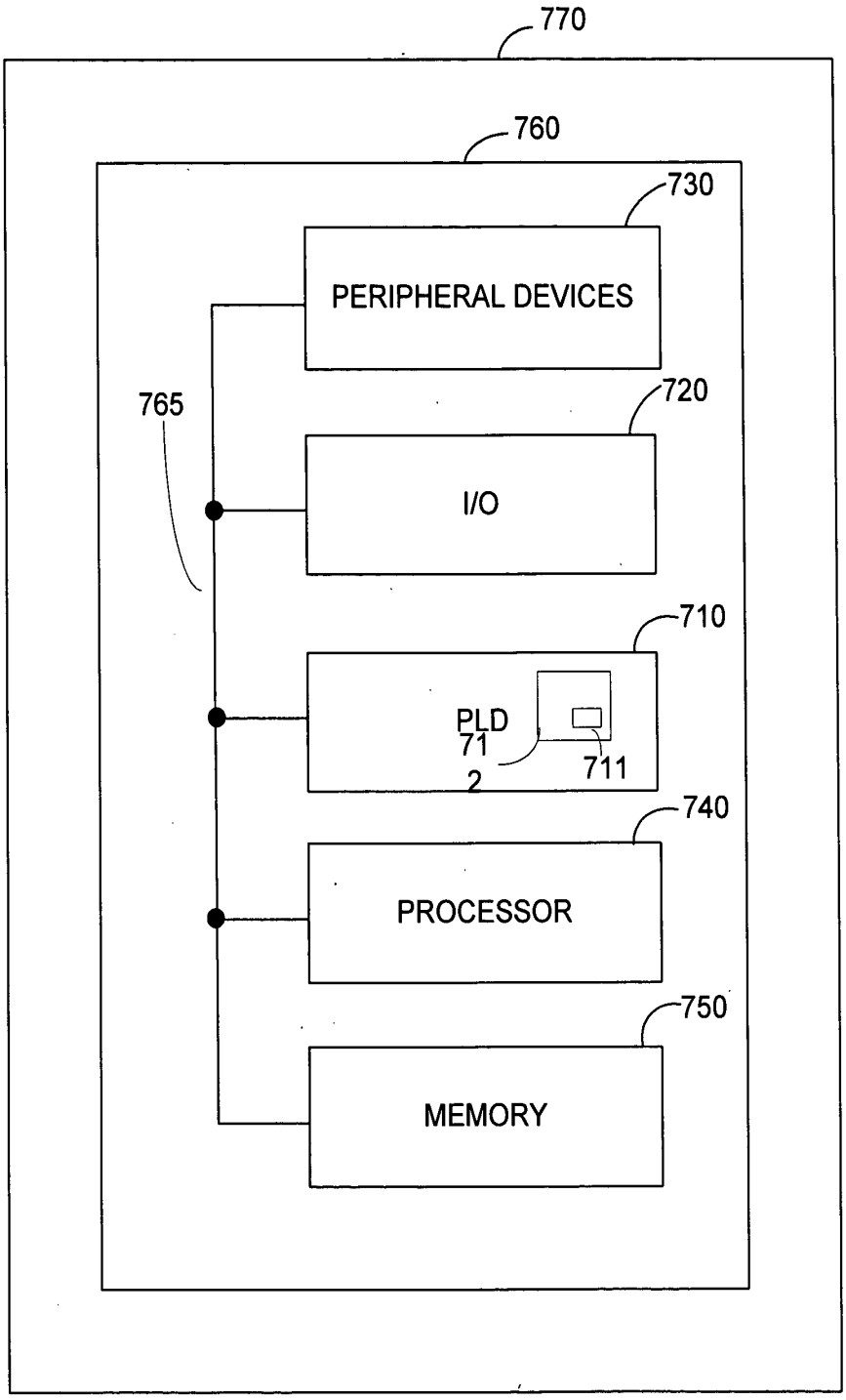



**FIG. 9. Shared Lookup-Table Mapping Circuitry with Zero-able input**


770
760
730
PERIPHERAL DEVICES
765
720
I/O
710
PLD
71
2
711
740
PROCESSOR
750
MEMORY

700

FIG. 10